

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		09989777
	Filing Date		2001-11-19
	First Named Inventor	Craig Nemecek	
	Art Unit	2123	
	Examiner Name	Mary C. Jacob	
	Attorney Docket Number	CD01208M	

U.S. PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	7042301	B1	2006-05-09	Sutardja, Sehat	Entire Document
	2	5594388	B1	1997-01-14	O'Shaughnessy et al.	Entire Document
	3	5963105	B1	1999-10-05	Nguyen	Entire Document
	4	5982241	B1	1999-11-09	Nguyen et al.	Entire Document
	5	6133773	B1	2000-10-17	Garlepp et al.	Entire Document
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	8	6973400	B1	2005-12-06	Cahill-O'Brien et al.	Entire Document

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9	7129793	B1	2006-10-31	Gramegna	Entire Document
10	7250825	B1	2007-07-31	Wilson et al.	Entire Document
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15	6809566	B1	2004-10-26	Xin-LeBlanc, Jane	Entire Document
16	6154064	B1	2000-11-28	Proebsting, Robert J.	Entire Document
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18	4326135	B1	1982-04-20	Jarrett et al.	Entire Document
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21	5432476	B1	1995-07-11	Tran	Entire Document
22	5929710	B1	1999-07-27	Bien	Entire Document
23	5945878	B1	1999-08-31	Westwick et al.	Entire Document
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39	5764714	B1	1998-06-09	Stansell et al.	Entire Document
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43	6026134	B1	2000-02-15	Duffy et al.	Entire Document
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FOREIGN PATENT DOCUMENTS

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	1	Application Number 11/850,260 (CD2007006): "Circuit and Method for Improving the Accuracy of a Crystal-less Oscillator Having Dual-Frequency Modes," Wright et al.; 33 pages	<input type="checkbox"/>
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	5	USPTO Final Rejection for Application Number 11/644,100 (CD05204) dated 11/18/2008; 12 pages	<input type="checkbox"/>

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6	USPTO Non-Final Rejection for Application Number 11/644,100 (CD05204) dated 04/14/2008; 10 pages	<input type="checkbox"/>
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29	Application Number 10/305,589 (CD02181): "Current Controlled Delay Circuit," Stiff; 18 pages	<input type="checkbox"/>
30	Application Number 09/849,164 (CD01035): "Reduced Static Phase Error CMOS PLL Charge Pump," Stiff, 30 pages	<input type="checkbox"/>
31	Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, 10 pages	<input type="checkbox"/>
32	Larsson, "A 2-1600-MHz CMOS Clock Recovery PLL with Low-V _{dd} Capability," IEEE Journal of Solid-State Circuits, Vol. 34, No. 12, December 1999, 10 pages	<input type="checkbox"/>
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38	USPTO Final Rejection for Application Number 10/871,582 (CD03036) dated 02/01/2006; 5 pages	<input type="checkbox"/>

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40	Application Number 10/871,582 (CD03036): "LVDS Input Circuit with Extended Common Mode Range," Reinschmidt et al.; 25 pages	<input type="checkbox"/>
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46	USPTO Non-Final Rejection for Application Number 09/404,891 (CD99054) dated 03/05/2003, 6 pages	<input type="checkbox"/>
47	USPTO Non-Final Rejection for Application Number 09/404,891 (CD99054) dated 10/11/2002, 5 pages	<input type="checkbox"/>
48	Application Number 09/404,891 (CD99054): "Method, Architecture and Circuitry for Controlling Pulse Width in a Phase and/or Frequency Deflector," Scott et al.; 17 pages	<input type="checkbox"/>
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